UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Haritsa	SUN-P5403	7441

7590 02/27/2003

David B. Ritchie
Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640

EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,452	HARITSA ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/982452 filed on 10/17/01.

Claims 1-77 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Naganuma et al. (U.S Patent 5917729).

3. As to claim 1 (method), 16 (apparatus), 31 (apparatus), and 43 (computer readable medium), Naganuma et al. teaches a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 5 col 7 lines 54-57 and fig 15 col 10 lines 20-23); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net (see fig1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 23-53); and combining the plurality of simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

4. As to claims 2, 17, 32 and 44, Naganuma et al. teaches wherein partitioning comprises breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates (see fig 2).

5. As to claims 3, 18, 33, and 45 Naganuma et al. teaches further comprising breaking at least one of the plurality of local clock nets down into at least one sub-local clock net (see fig 15 and fig 16).

6. As to claim 4, 19, 34 and 46, Naganuma et al. teaches further comprising simulating the at least one sub-local clock net prior to simulating the corresponding local clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

7. As to claims 5, 20, 35, and 47, Naganuma et al. teaches wherein at least two of the plurality of local clock nets are simulated in parallel (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

8. As to claims 6, 21, 36, and 48, Naganuma et al. teaches wherein simulating each of the plurality of local clock nets comprises: extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41); extracting component values of the elements of the local clock net from the microprocessor network database (see fig 1 element ST10 and fig29 element ST20 and ST13 col 12 lines 35-41); simulating the local clock net based on the layout and the component values (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); and extracting a load of the local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

9. As to claims 7, 22, 37, and 49, Naganuma et al. teaches wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

10. As to claims 8, 23, 38, and 50, Naganuma et al. teaches wherein simulating the global clock net comprises: extracting the layout of the global clock net from a microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41 and col 10 lines 23-53); extracting component values of the elements of the global clock net from the microprocessor network database (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41 and col 10 lines 23-53); inserting the simulated loads of the plurality of local clock nets (see fig 1 element ST10 and fig 29 element ST20 and ST13 col 12 lines 35-41); and simulating the global clock net based on the layout, the component values, and the simulated local clock net loads (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

11. As to claims 9, 24, 39, and 51, Naganuma et al. teaches further comprising storing the plurality of simulation results in a Clock Data Model (see col 12 lines 50-55).

12. As to claims 10, 25, 40, and 52, Naganuma et al. teaches further comprising evaluating the complete clock net to determine whether the results converge (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

13. As to claims 11, 26, 41, and 53, Naganuma et al. teaches wherein, if the results do not converge, the method further comprises: assuming that clock arrival times are those calculated for the simulated global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col

12 lines 35-41); re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41); and combining the simulations and re-simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 12 lines 35-41).

14. As to claims 12, 27, and 54, Naganuma et al. teaches wherein re-simulating at least one of the plurality of local clock nets comprises: re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 35-41); and extracting a load of the at least one local clock net on the global clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 35-41).

15. As to claims 13, 28, and 55, Naganuma et al. teaches further comprising re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68).

16. As to claims 14, 29, and 56, Naganuma et al. teaches wherein re-simulating the global clock net comprises: inserting the simulated or re-simulated loads of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41); and re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

17. As to claims 15, 30, 42, and 57, Naganuma et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

18. As to claims 58 (method), 63 (apparatus), 68 (apparatus), and 733 (computer readable medium), Naganuma et al. teaches a method of determining and analyzing clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 5 col 7 lines 54-57 and fig 15 col 10 lines 20-23); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net (see fig1 element ST10 and fig29 element ST21 and ST13 col 10 lines 55-68); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 1 element ST10 and fig29 element ST21 and ST13 col 10 lines 23-53); combining the plurality of simulations to form the complete clock net (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41); and analyzing the complete clock net to predict the clock skew for a given data transfer path (see col 7 lines 65 –67 and col 8 lines1-6 and col 11 lines 1-12).

19. As to claims 59, 64, 69, and 74, Naganuma et al. teaches wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer path (see col 10 lines 10-14 and col 10 lines 33-42); and re simulating at least one local clock net involved in the given data transfer path (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

20. As to claims 60, 65, 70, and 75, Naganuma et al. teaches further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

21. As to claims 61, 66, 71, and 76, Naganuma et al. teaches further comprising evaluating the at least one re-simulated clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

22. As to claims 62, 67, 72, and 77, Naganuma et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 1 element ST10 and fig29 element ST21 and ST11-14 col 12 lines 36-41).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art Unit 2825
February 22, 2003

LEON M. GOLDSTEIN
PATENT EXAMINER